FIG.1

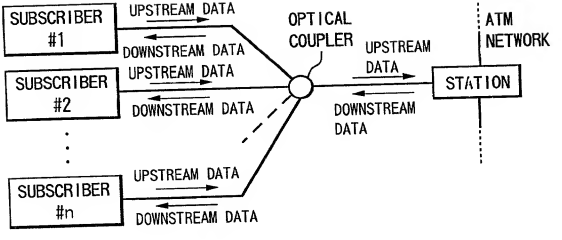


FIG.2A

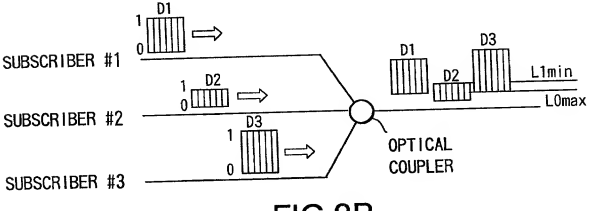


FIG.2B

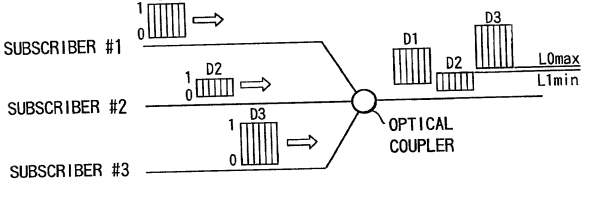


FIG.3

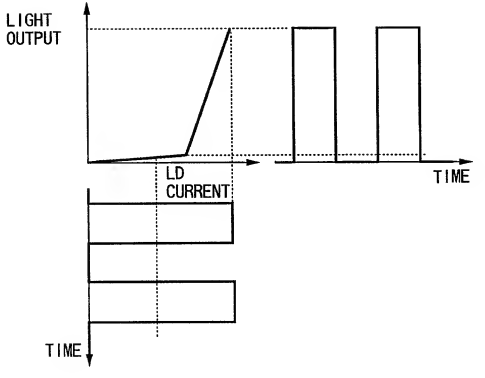

LIGHT
OUTPUT
LD
CURRENT
TIME
TIME

FIG.4

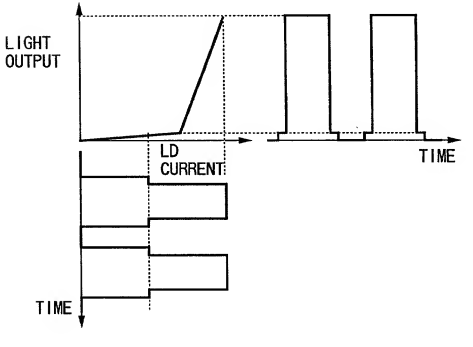

LIGHT
OUTPUT
LD
CURRENT
TIME
TIME

FIG.5

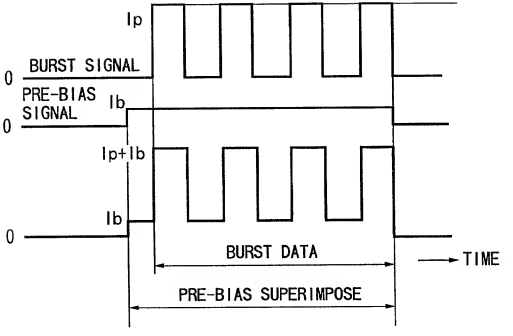

Ip
BURST SIGNAL
0
PRE-BIAS SIGNAL
Ib
0
Ip+Ib
Ib
0
BURST DATA
TIME
PRE-BIAS SUPERIMPOSE

FIG.6

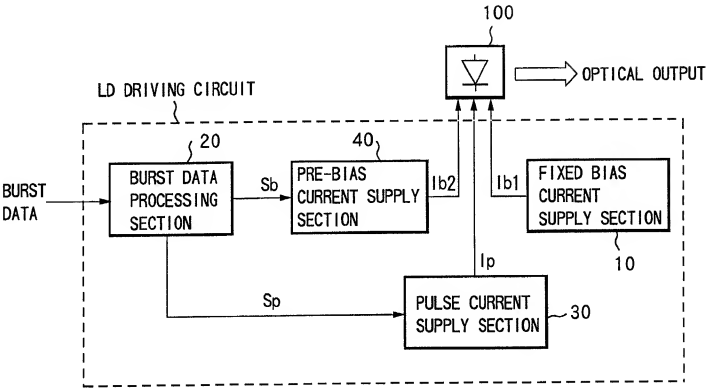

100
OPTICAL OUTPUT
LD DRIVING CIRCUIT
20
40
BURST DATA PROCESSING SECTION
Sb
PRE-BIAS CURRENT SUPPLY SECTION
Ib2
Ib1
FIXED BIAS CURRENT SUPPLY SECTION
10
BURST DATA
Ip
Sp
PULSE CURRENT SUPPLY SECTION
30

FIG.7

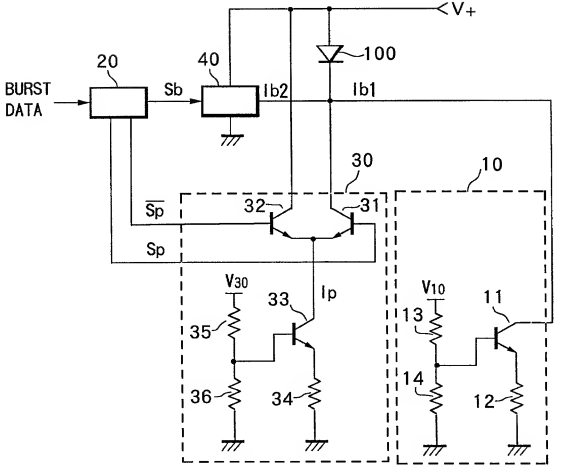

V+
100
20
40
BURST
DATA
Sb
Ib2
Ib1
30
10
Sp
32
31
Sp
V30
33
Ip
V10
11
13
35
14
36
34
12

FIG.8

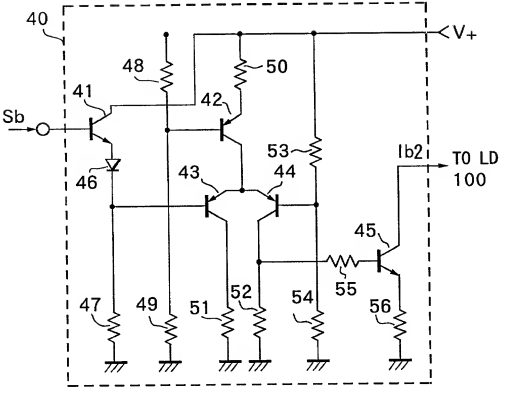

40
V+
48
50
41
42
Sb
53
Ib2
TO LD
100
46
43
44
45
55
47
49
51
52
54
56

FIG.9

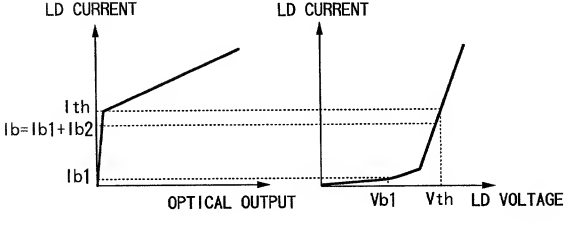

LD CURRENT
LD CURRENT
Ith
Ib=Ib1+Ib2
Ib1
OPTICAL OUTPUT
Vb1
Vth
LD VOLTAGE

FIG.10

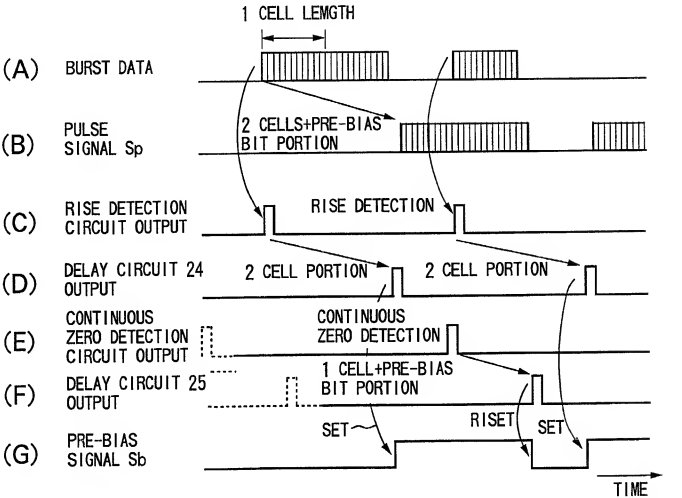

1 CELL LEMGTH
(A)
BURST DATA
(B)
PULSE
SIGNAL Sp
2 CELLS+PRE-BIAS
BIT PORTION
(C)
RISE DETECTION
CIRCUIT OUTPUT
RISE DETECTION
(D)
DELAY CIRCUIT 24
OUTPUT
2 CELL PORTION
2 CELL PORTION
(E)
CONTINUOUS
ZERO DETECTION
CIRCUIT OUTPUT
CONTINUOUS
ZERO DETECTION
(F)
DELAY CIRCUIT 25
OUTPUT
1 CELL+PRE-BIAS
BIT PORTION
(G)
PRE-BIAS
SIGNAL Sb
SET
RISET
SET
TIME

FIG.11

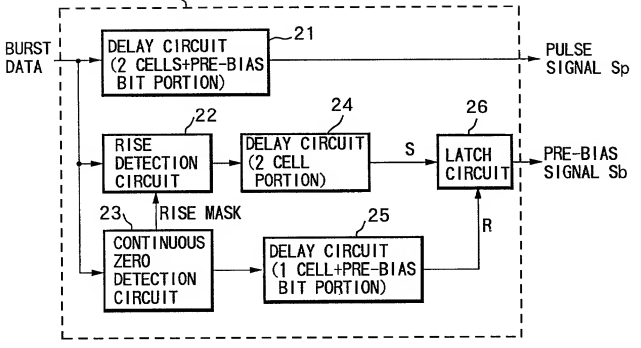

20
BURST DATA
DELAY CIRCUIT (2 CELLS+PRE-BIAS BIT PORTION)
21
PULSE SIGNAL Sp
22
RISE DETECTION CIRCUIT
24
DELAY CIRCUIT (2 CELL PORTION)
S
26
LATCH CIRCUIT
PRE-BIAS SIGNAL Sb
23
RISE MASK
CONTINUOUS ZERO DETECTION CIRCUIT
25
DELAY CIRCUIT (1 CELL+PRE-BIAS BIT PORTION)
R

FIG.12

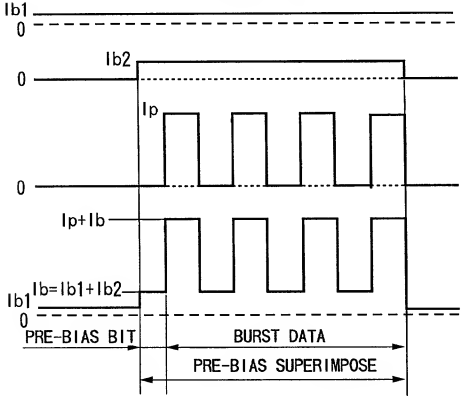

Ib1
0
Ib2
0
Ip
0
Ip+Ib
Ib=Ib1+Ib2
Ib1
0
PRE-BIAS BIT
BURST DATA
PRE-BIAS SUPERIMPOSE

FIG.13

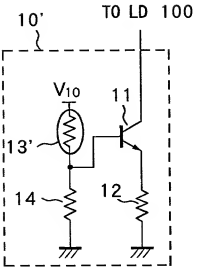

10'
TO LD 100
V_{10}
11
13'
14
12

FIG.14

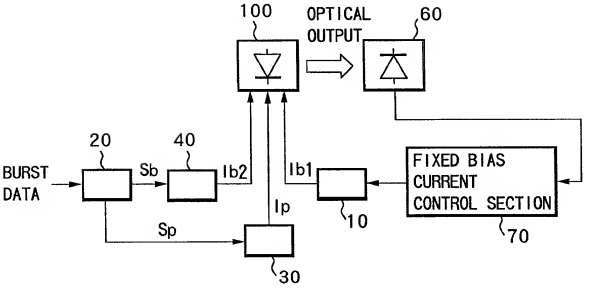

100
OPTICAL OUTPUT
60
20
40
BURST DATA
Sb
Ib2
Ib1
FIXED BIAS CURRENT CONTROL SECTION
Ip
10
Sp
70
30

FIG.15

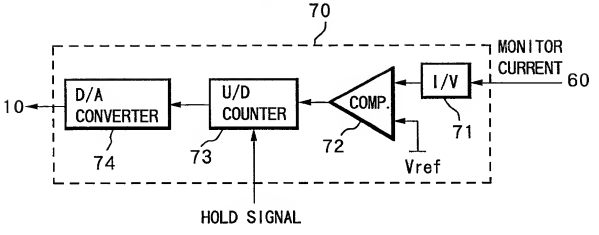

70
MONITOR CURRENT
60
I/V
71
COMP.
72
Vref
U/D COUNTER
73
D/A CONVERTER
74
10
HOLD SIGNAL

FIG.16

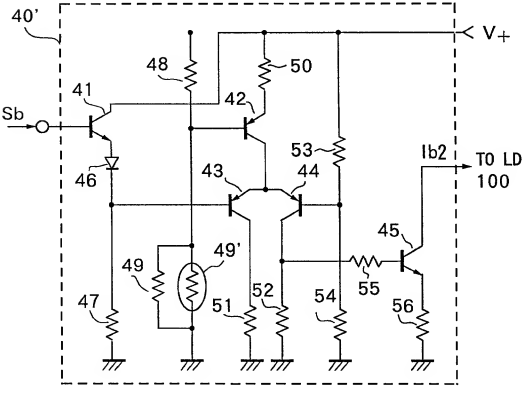

40'
V+
48
50
41
42
Sb
46
53
43
44
Ib2
TO LD 100
45
49
49'
55
47
51
52
54
56

FIG.17

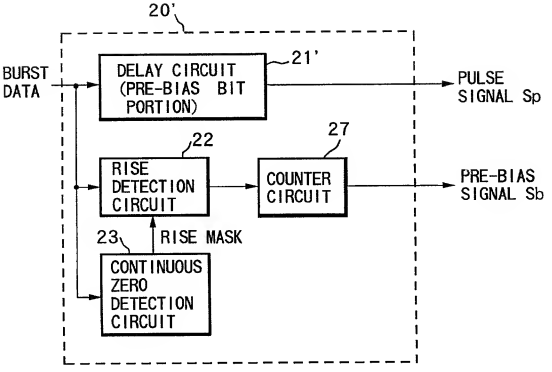

20'
BURST DATA
DELAY CIRCUIT (PRE-BIAS BIT PORTION)
21'
PULSE SIGNAL Sp
22
RISE DETECTION CIRCUIT
27
COUNTER CIRCUIT
PRE-BIAS SIGNAL Sb
23
RISE MASK
CONTINUOUS ZERO DETECTION CIRCUIT

FIG.18

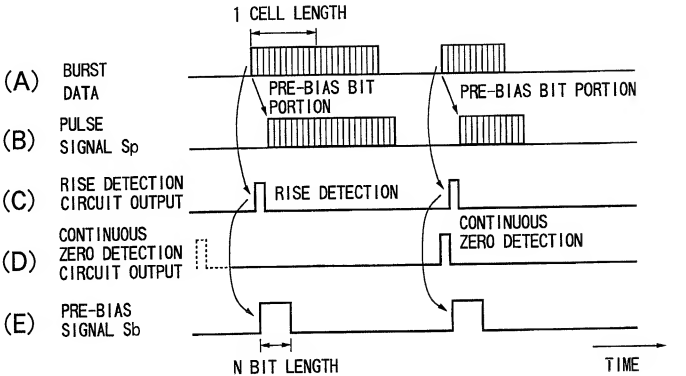

1 CELL LENGTH
(A)
BURST DATA
PRE-BIAS BIT PORTION
PRE-BIAS BIT PORTION
(B)
PULSE SIGNAL Sp
(C)
RISE DETECTION CIRCUIT OUTPUT
RISE DETECTION
(D)
CONTINUOUS ZERO DETECTION CIRCUIT OUTPUT
CONTINUOUS ZERO DETECTION
(E)
PRE-BIAS SIGNAL Sb
N BIT LENGTH
TIME

FIG.19

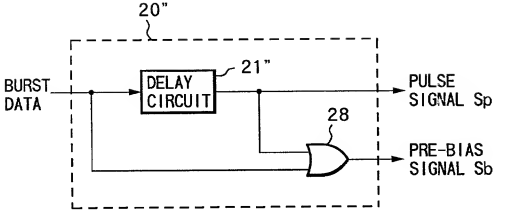

20"
BURST DATA
DELAY CIRCUIT
21"
28
PULSE SIGNAL Sp
PRE-BIAS SIGNAL Sb

FIG.20

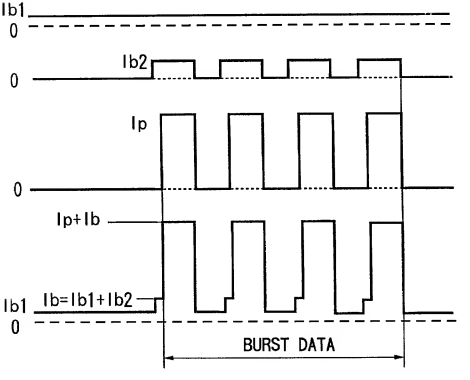
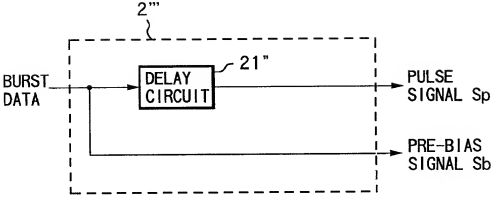

Ib1
0
Ib2
0
Ip
0
Ip+Ib
Ib1
Ib=Ib1+Ib2
0
BURST DATA

FIG.21


2'''
21"
BURST
DATA
DELAY
CIRCUIT
PULSE
SIGNAL Sp
PRE-BIAS
SIGNAL Sb